An Integrated Architectural Clock Implemented Memory Design Analysis

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***Abstract*—Recently Low power consumption and Custom Memory design is major issue for embedded designer. Micro wind and Xilinx simulator implements SRAM design architecture and performs efficient simulation. These simulators implements high performances and low power consumption of SRAM design. SRAM efficiency analyzed with 6-T architecture design and row/column based architectural design. We have analyzed clock implemented memory design and simulated with specific application. We have implemented clock based SRAM architecture that improves the internal clock efficiency of SRAM. Architectural Clock implemented memory design reduces the propagation delay and access time. Internal semiconductor material design implemented technique also improves the SRAM data transitions scheme. Semiconductor material and clock implemented design improve simulation performance of SRAM and these design implements for recently developed Application Specific Memory Design Architecture and mobile devices.**

Keywords—SRAM Architecture; Simulation; Micro wind; Xilinx; Clock Implemented Memory Design; RTL Design

I. INTRODUCTION

Custom architecture design analyzes the behavior of memory implements for high performance and low power consumption. Various simulators implements High performance and they simulate cache design in various structures. We have used some simulators such as micro wind, Xilinx. By the help of these simulators we implements memory structure in various formats. Micro wind simulator used to design architectural memory cell and simulates an integrated circuit. It's contains a library of common logic and analog ICs to view and simulate logic circuits.

Electric extraction of this circuit is automatically performs analog simulation curve immediately. A sense amplifier is used to read the contents of SRAM cells and performs the amplification, delay reduction and power reduction. Sense amplifier plays dominant role in SRAM cell architecture and used to sense the stored data. Xilinx simulator used to verify the functionality and timing of integrated circuit designs. Xilinx simulation process is allowed as to creating and verifying complex circuit's functions. Recently transistor technology increases the SRAM capability usually 6-12 transistors used for high performance but the cell size is gradually increases is the major issue. The no. of transistors can be reduces and implements clock and materials design techniques that reduces data losses of SRAM.

A cell design architecture implementation method improves the SRAM performance and consumes low power. Cache implementation technique also implements high speed data transfer scheme. Kuldar at el. [1] proposed a technique to synthesize the local memory architecture of a clustered accelerator using a phase-ordered approach. Merolla at el. [2] designed fabricated key building block of neurosynaptic core, with 256 digital integrated neurons and 1024x256 bit SRAM crossbar memory design architecture. Panda at el. [3] proposed scratch-pad memory architecture design for application specific processor and used optimization technique to customize embedded system. Park and Diniz [4] designed Static RAM and synchronous Dynamic RAM with efficient latency and access modes. The synthesis methods implement the advanced memory structure, such as "smart buffer", that require recovery of additional high-level information about loops and array [5]. Sense amplifier designs improve sensing delay and it's performs excellent tolerance to process variations [7]. Three novel cache models [9] using Multiple-Valued Logic (MVL) to reduces the cache data storage area and cache energy consumption for embedded systems. Spin-transfer torque RAM (STT-RAM) [10] is an emerging nonvolatile Memory technology that used low-power and high-density advantages over the SRAM.

Calhaun and Chandrkasan [11] proposed low-voltage operation technique for traditional transistor (6 t) SRAM. Dhanumjaya at el. [12] presented the dynamic column based power supply of 8T SRAM cell design and these architecture design is implements with conventional SRAM 6T in various aspects. Chen at el. [13] compared of 6T and 8T bit cell design in various domains with specific condition. Shukla at el. [14] presented a novel structure of the SRAM Bit-Cell, called as P4-SRAM Bit-Cell structure. These proposed bit-cells utilizes the Gated-VDD technique for transistor stacking in the PP-SRAM along with the full-supply body biasing to reduce the active, standby, and dynamic power in the memory. Dadoria at el. [15] analyzed the comparison of different type of SRAM topology, at 180nm CMOS technology that improves stability, power dissipation and performance.

II. Architectural SRAM Design

Static SRAM cell implements with access transistors and these access transistor implements memory operations.6-T Static SRAM design architecture implemented with PN diffusion, data unit, and bit line by the help of Micro wind [Fig. 1 & Fig. 2]. Micro wind [8] simulator used to design and simulate SRAM architecture. SRAM Simulation speed depends upon the semiconductor material design and metal-contact mechanism [Fig. 3]. Internal architecture of Static SRAM [Fig. 4] material design contains Silicide material and this Silicide also implemented with Salicide (oxide implemented silicide) material. This Semiconductor material design improves the SRAM capability and reduces the gap of p-n substrates. We have analyzed 4 sets of 6-T SRAM design with Salicide (oxide implemented silicide) material and these materials implement data transition speed and access time [Fig. 5] in efficient manner. SRAM contains Sense amplifier unit that used to sense stored the data. SRAM capability also implements with clock design mechanism. By the help of Micro wind we have analyzed internal architecture of SRAM and analyzed the clock based SRAM architecture [Fig. 6]. SRAM cell design implemented with row and column based 64-T architecture and Sense amplifier unit.

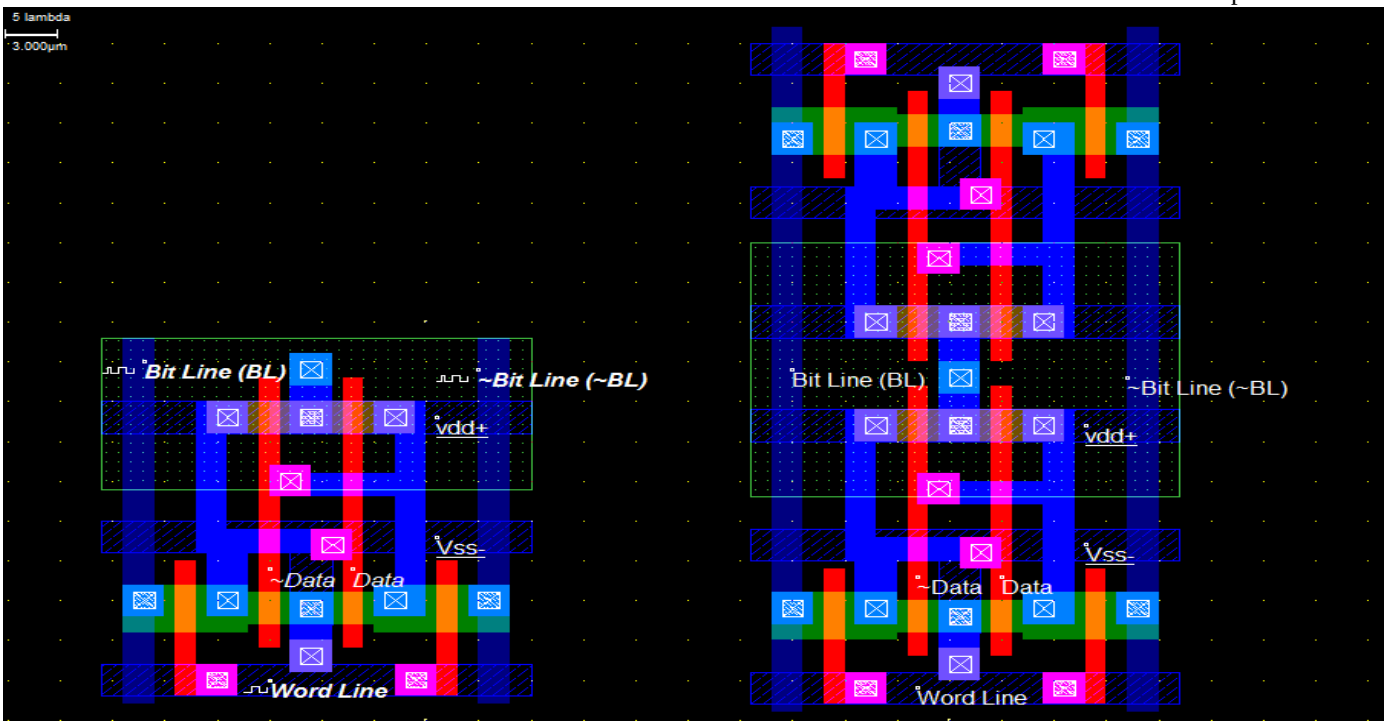

Fig. 1. CMOS 6-T SRAM Circuit structure

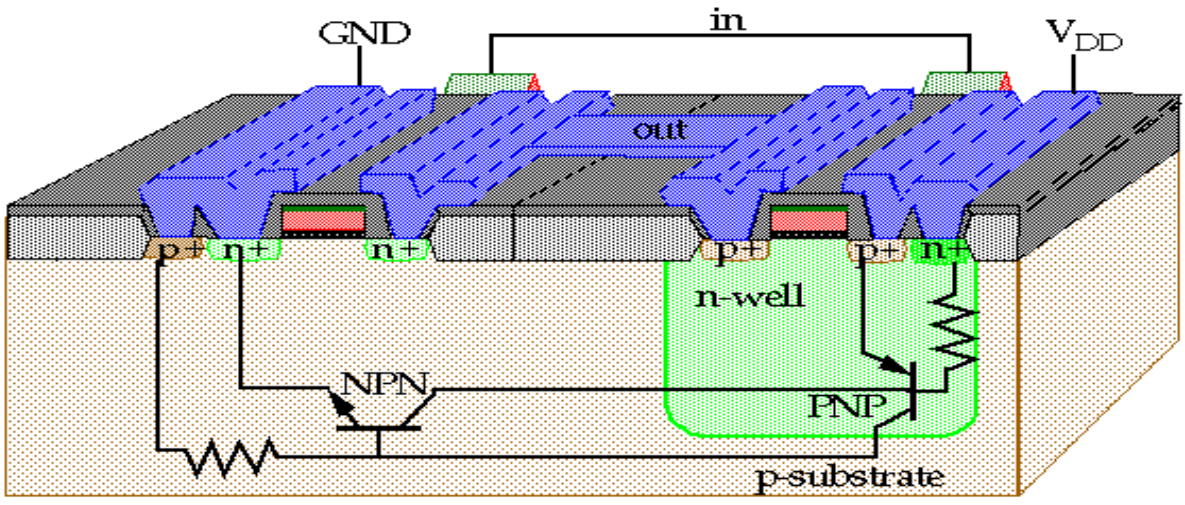

Fig. 2. Basic internal architecture of CMOS SRAM

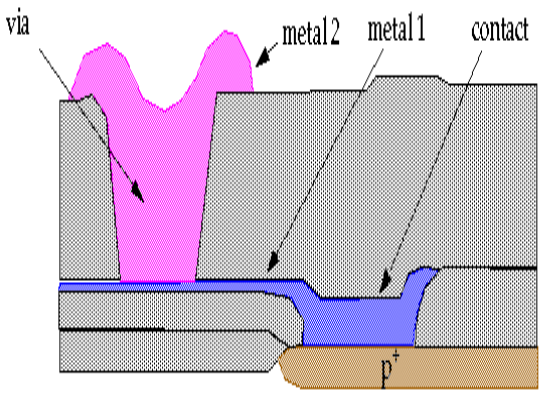

Fig. 3. Metal contacted SRAM cell design

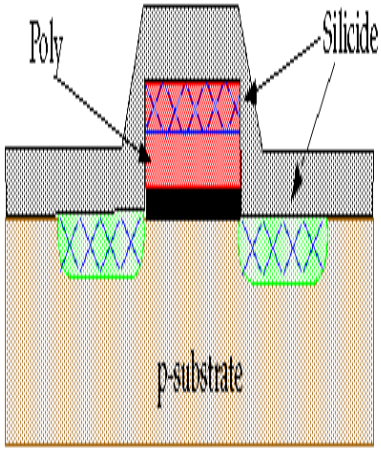

Fig. 4. Silicide material in SRAM cell

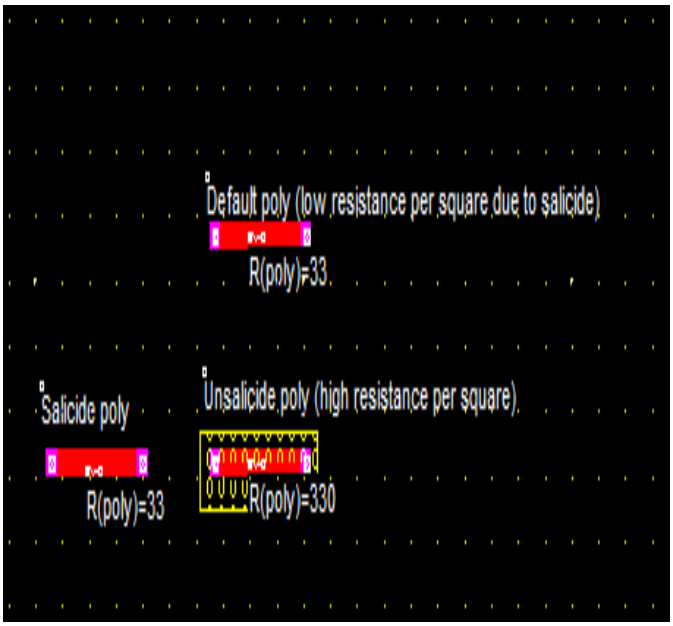

Fig. 5. Salicide material analysis in SRAM cell

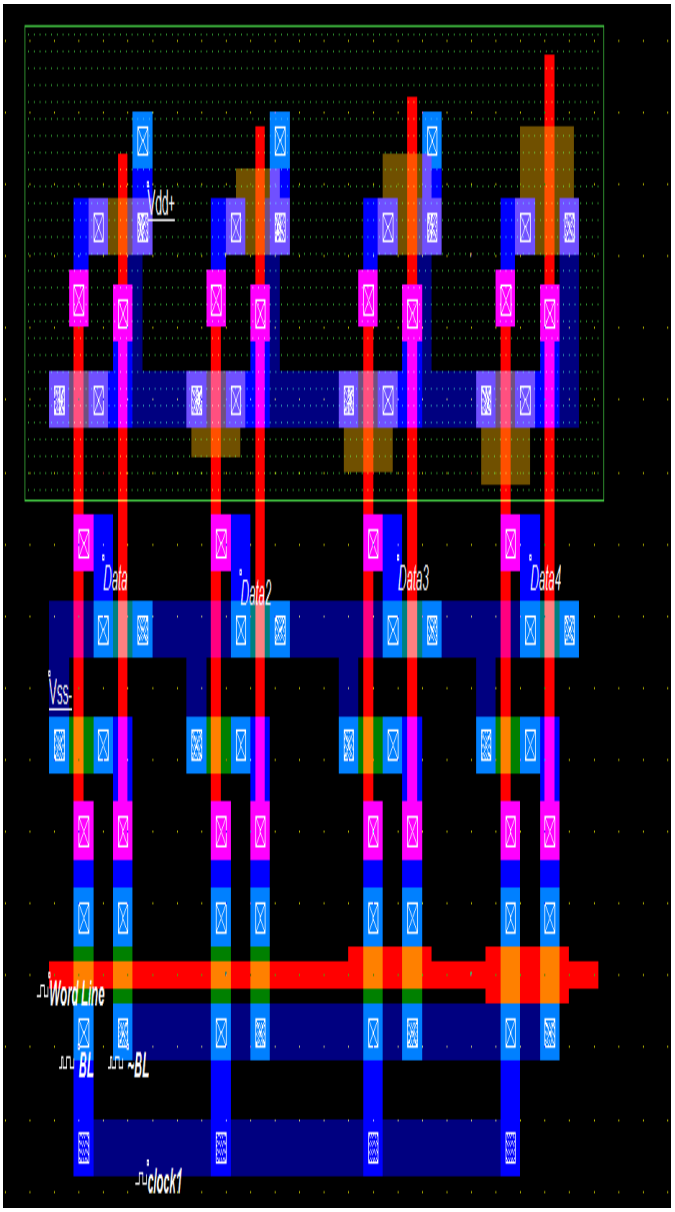

Fig. 6. Clock based SRAM design architecture

A. *Sense Amplifier*

Sense amplifier used to generate the low power signals from a bit line that stored in the Memory cell and amplifies with small voltage swing to recognizable Logic levels data are easily interpreted. The sense-amplifier circuits is usually consist of 4 to 6 Transistors and single sense amplifier unit associate with each column of memory cells, there are usually thousands or millions of identical sense amplifiers used as performance improvements. We have improved sense amplifier circuit with silicide to Salicide material design. These materials improve SRAM capability and increased internal data transitions speed. Sense amplifier unit designs with data unit, sense unit and pre-charge unit etc. [Fig 7]. SRAM design architecture such as 4-T to 12-T depends upon sense amplification mechanism.

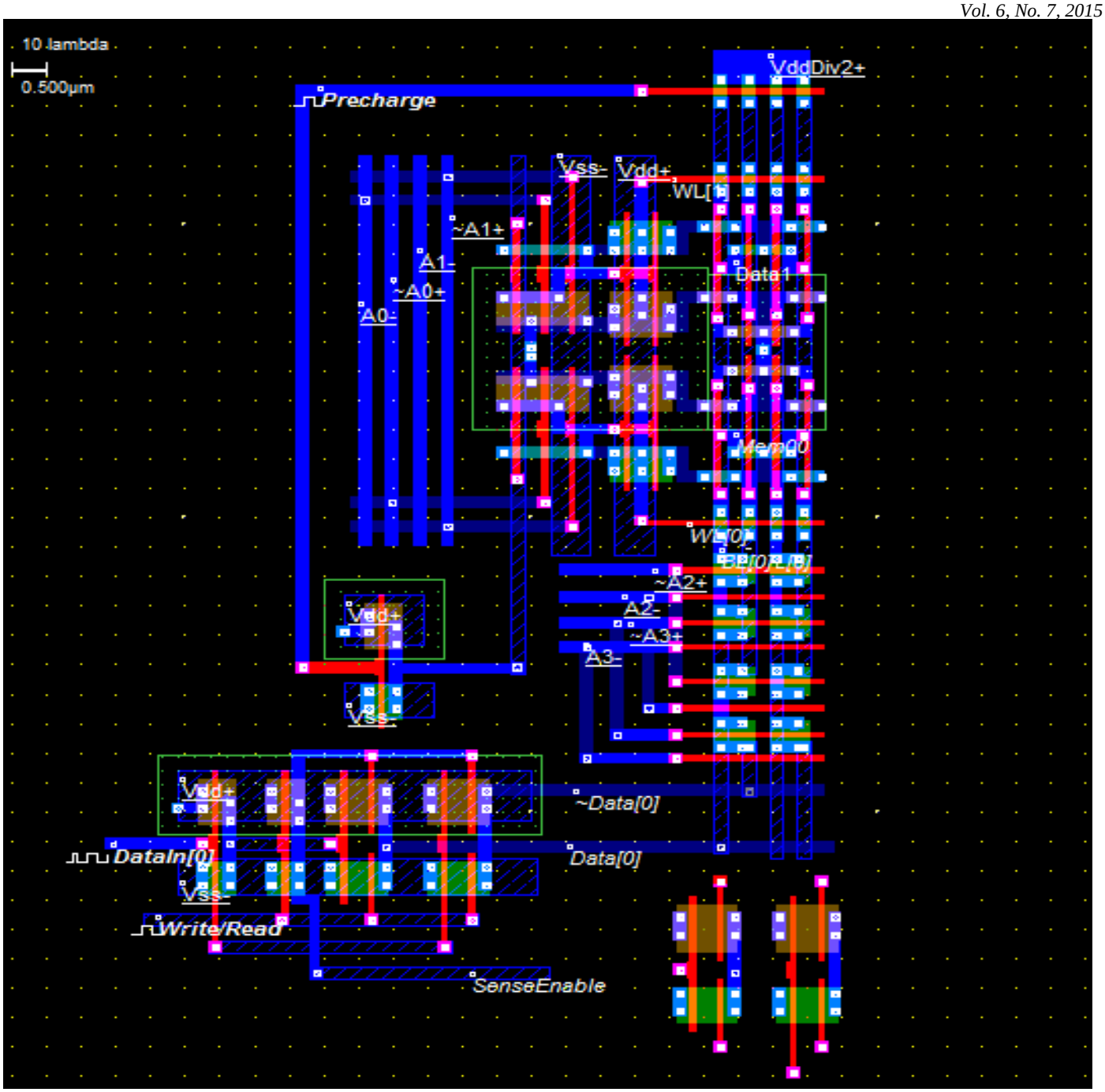

Fig. 7. Sense amplifier architectural design

B. *SRAM cell analysis for low power*

The 64-T Static SRAM design implements with access transistors. 64-T Static SRAM circuits design implements with sense amplifier unit that provides low power signals from a bit line is represents a data bit stored in a SRAM cell. We implements 64-T SRAM with Data IN unit, Data OUT unit, chip selection unit and sense amplifier circuits by the help of micro wind [Fig. 8]. When we have enabled the chip and sense amplifier it performs memory operation and produces the analogues result. We have implemented Salicide material quantity then it is gradually reduce the power consumption and performs efficient simulation. Salicide material improves simulation performance of SRAM with low power consumption and reduces the gap between P N substrate. We have implemented SRAM design with clocks [Fig. 6] and its internal cell design analysis with micro wind. We have also used Verilog code for RAM cell design analysis and implements clock by the help of Micro wind. SRAM design implements with row and column based 64-T cells and internal architecture decide efficient memory access pattern. SRAM Memory architecture implements with efficient clock mechanism by the help of Xilinx simulator [Fig. 9].

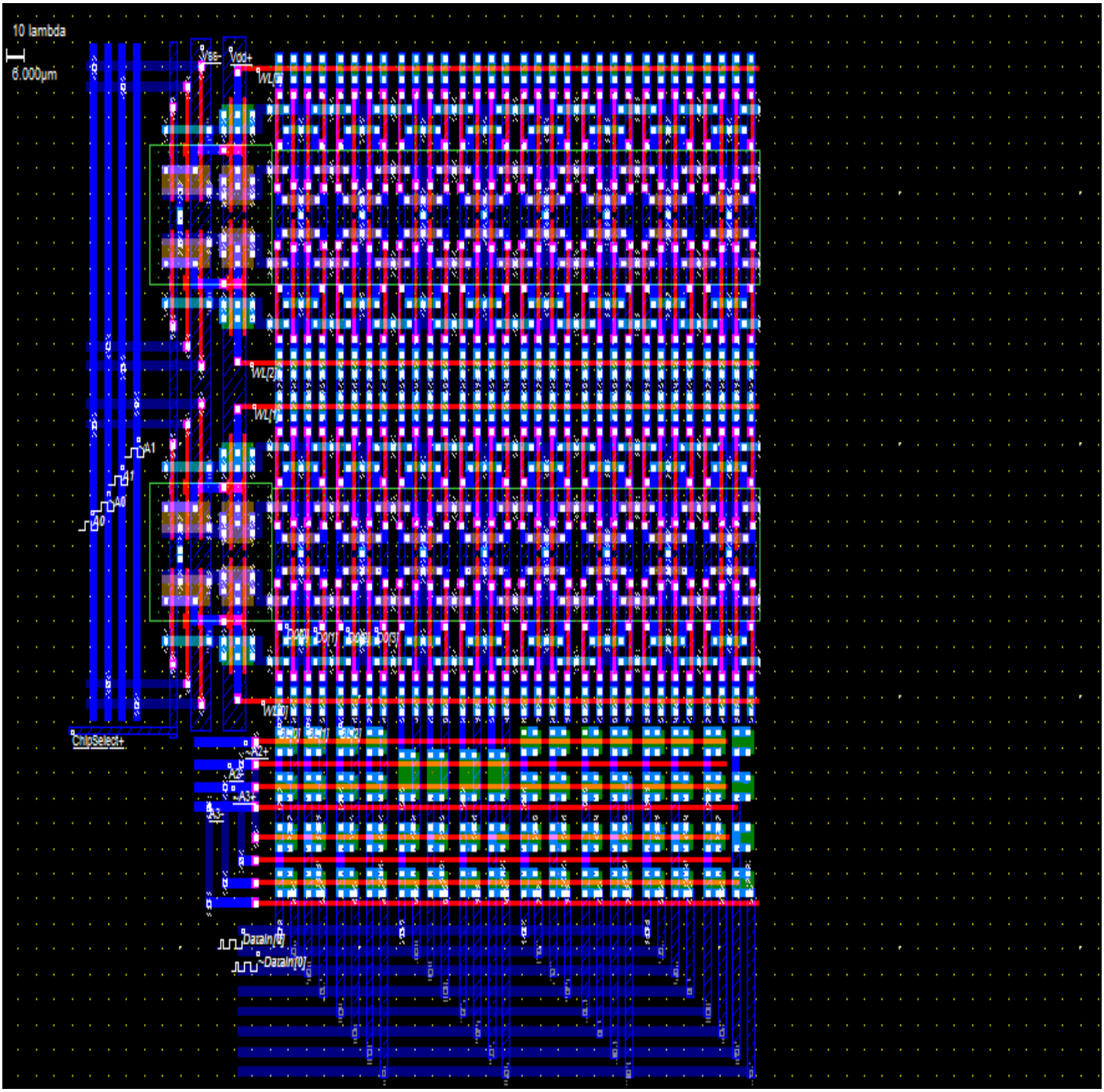

Fig. 8. Complex 64-T SRAM cell design

III. Clock Based Memory Architecture Design

Xilinx [6] simulator provides the interpretation of VHDL or VERILOG code into circuits functionally and performs the logic results of the HDL to determine circuit operations. During the HDL synthesis mechanism, XST analyzes the HDL code and attempts to imply the specific design building blocks. SRAM design implemented with clock, Clock controlling the write and read operation [Fig. 8].When writes enabled activated write address implements input data transfer and clock activated for write operations. When clock read is activated then it produces the output data and performs read operations. Clock implemented SRAM designs have synthesized with LUTs, mux, and buffer etc. [Fig. 9 and Fig. 10] by the help of Xilinx simulator.

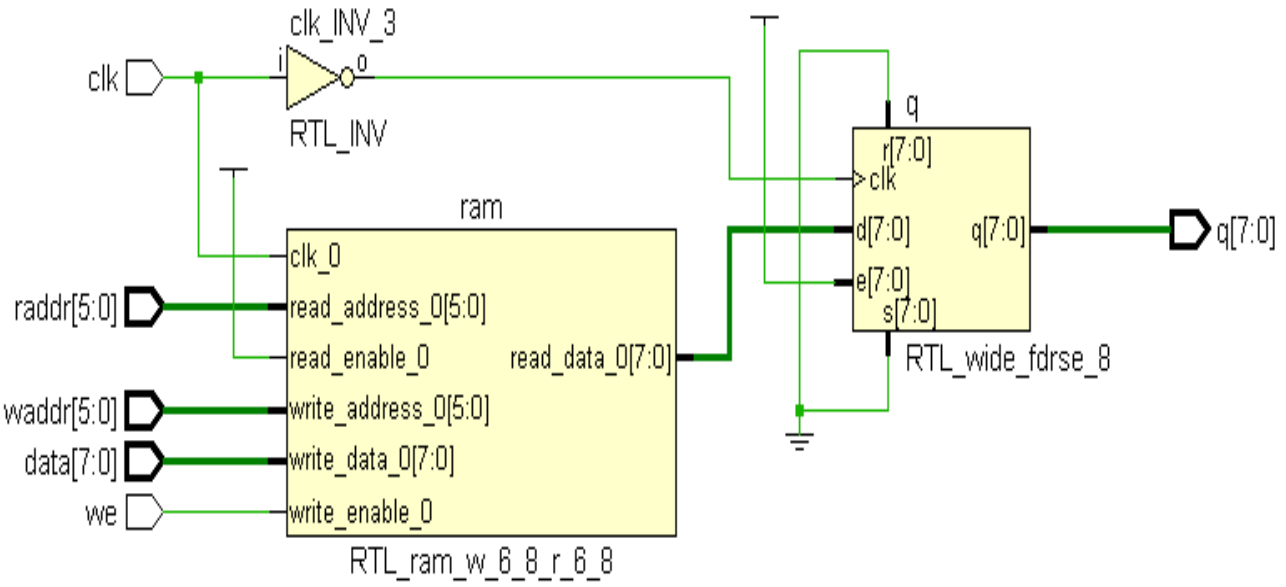

Fig. 9. SRAM cell design

A. *Dual Clock SRAM design*

Dual clock implemented cache design that implemented with separate read clocks and separate write clock when signal activated and performs memory operations. When write enabled then activated the write address for input data transfer and these separate write clock performs write operations. Another read clock signal is activated then it activates for read address and produces the output data and performs read operations. The Dual clock architectural of SRAM design implemented with ffd, buffer designs etc. [Fig.11 and Fig.12] and these dual clock design implements the data transitions scheme. These dual clocks SRAM design implements access time and reduces the propagation delay.

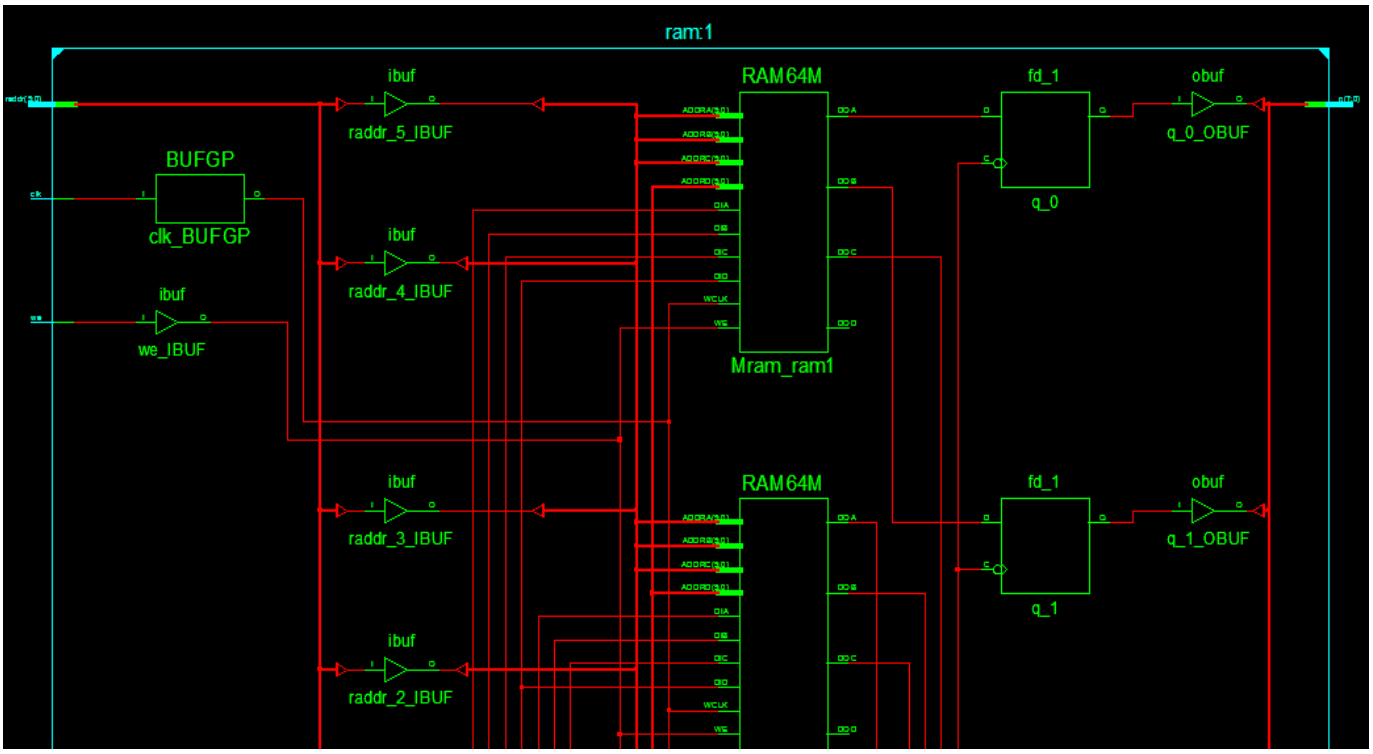

Fig. 10. RTL Design section of SRAM

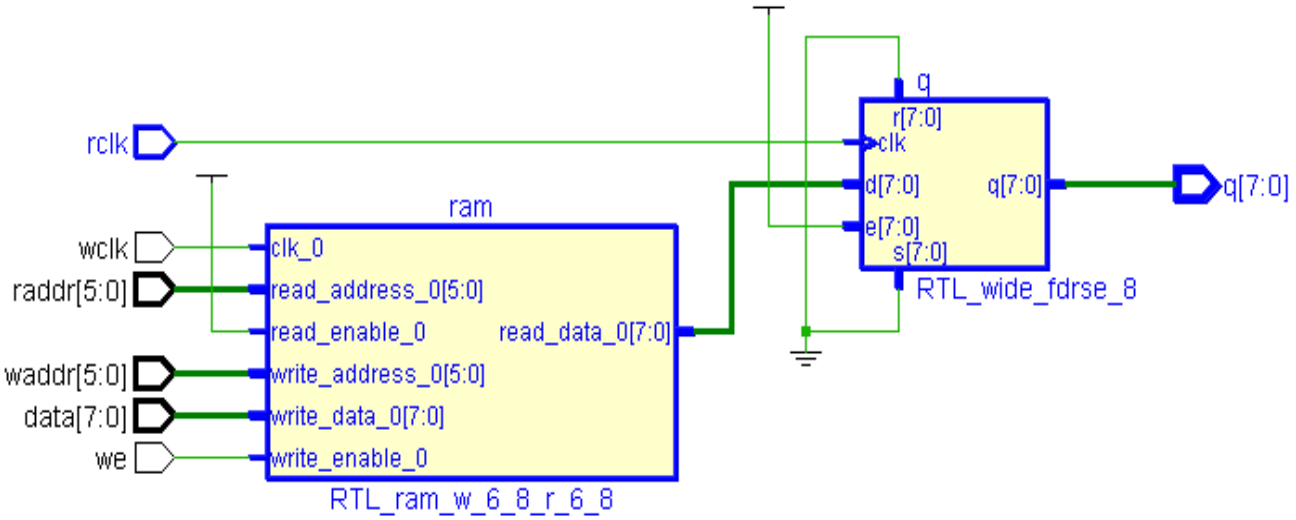

Fig. 11. Dual Clock SRAM Design

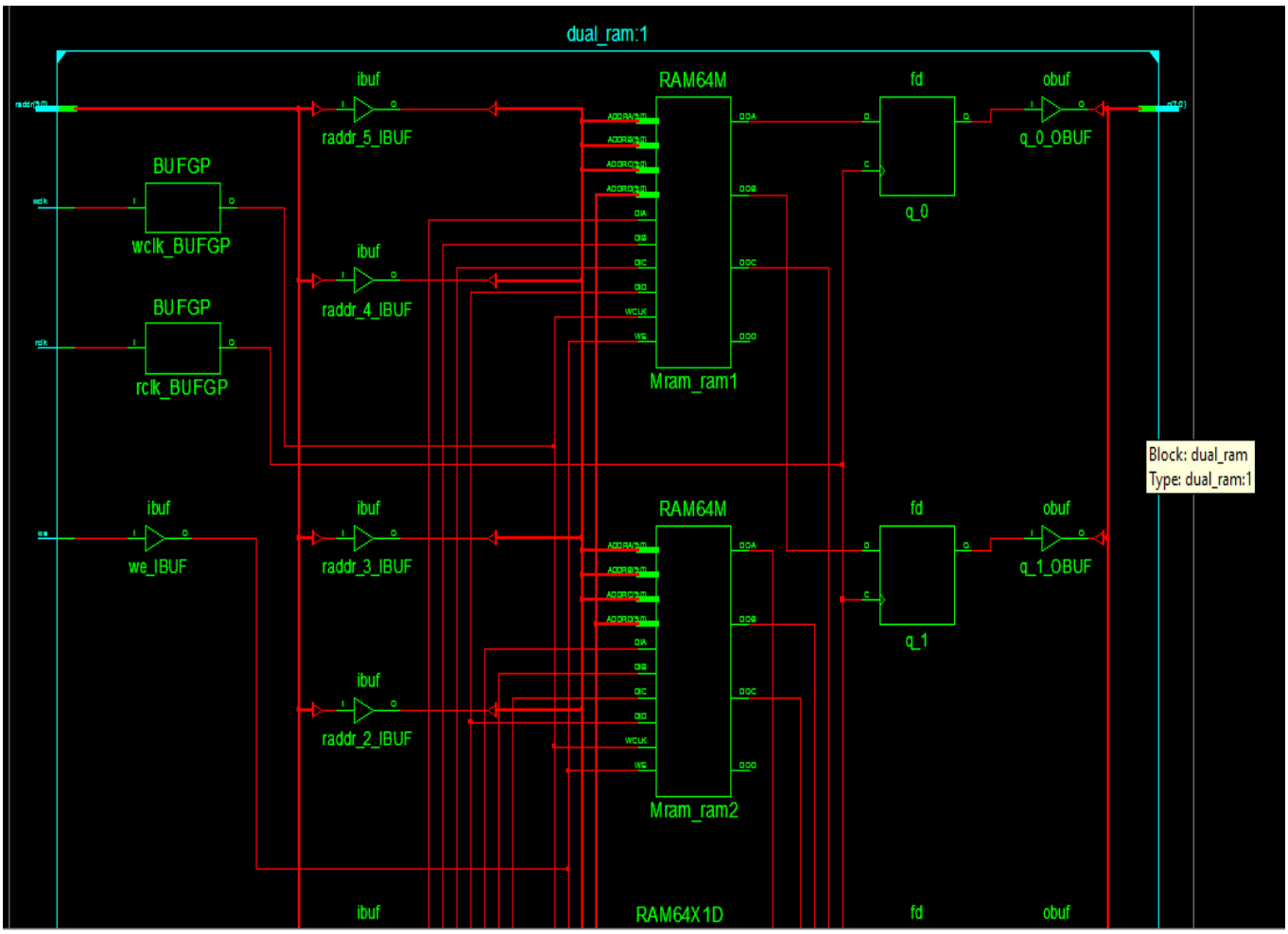

Fig. 12. Dual clock SRAM RTL Design section

B. Clock implemented SRAM Design

Clocks have implemented with subdivision mechanism and used counters are associated with a stream of ticks that represent time periods. Clock manage read and write operations with help of clock subdivision mechanism. Architectural clock based SRAM design implemented with counters, buffer etc. [Fig. 13 & Fig. 14]. Clock based counter used to manage all memory operation with schedule process and these architecture implements multiple data transitions scheme [Fig. 15].

Scheduled write/read operation reduces the data losses and implements memory access time and propagation delay time. We have analyzed that Single clock SRAM memory performs access time as 1ns and dual clock SRAM design implements simulation access time as 0.8ns because both operation implements data transitions with proper active state. Clock behavior implemented with clock subdivision mechanism and implements memory design that reduces the propagation delay time as 0.2ns or ten times reduces its depends upon clock edges pattern [Fig. 16 and Fig 17].

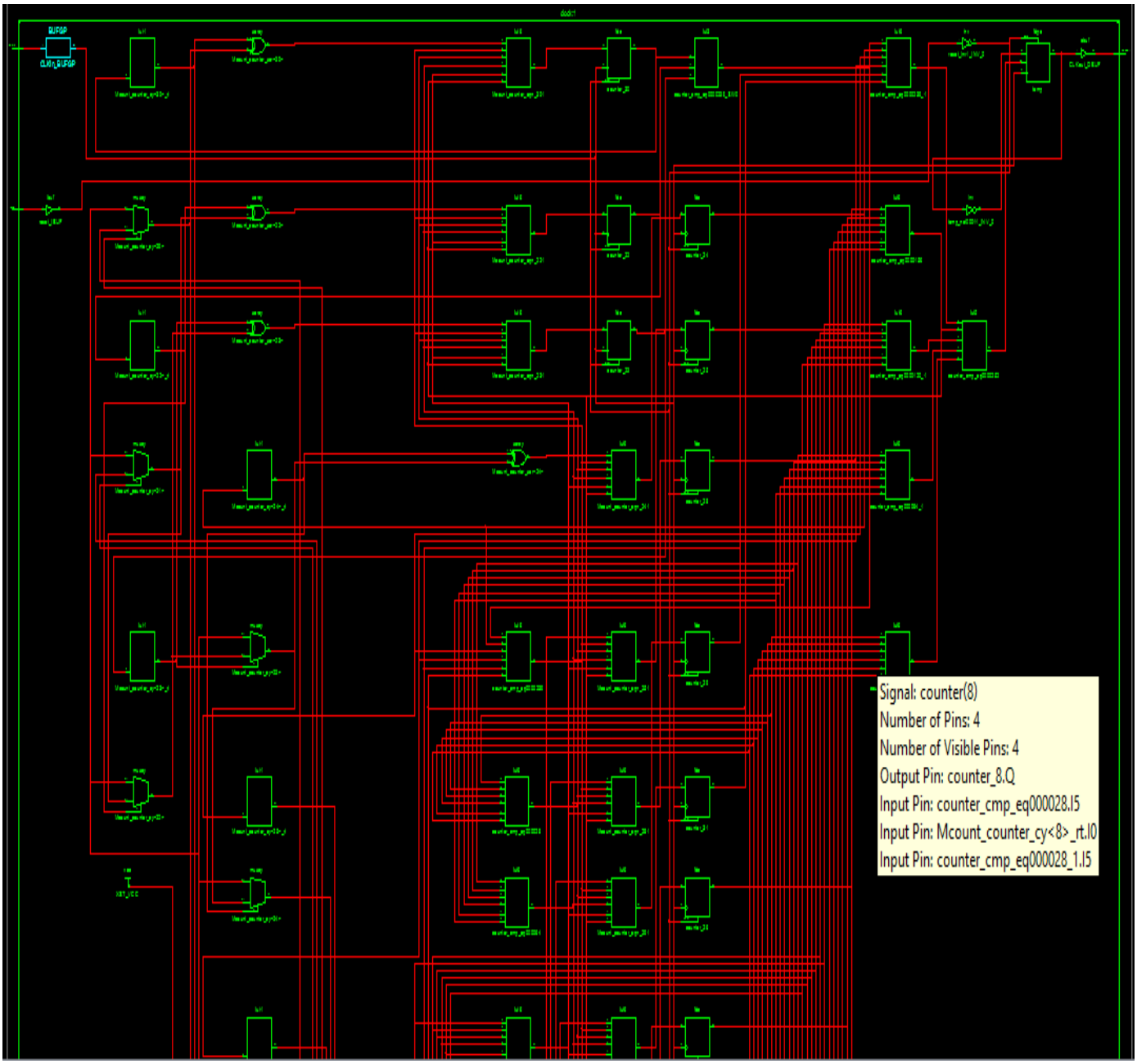

Fig. 13. Clock Implementation RTL design section of SRAM

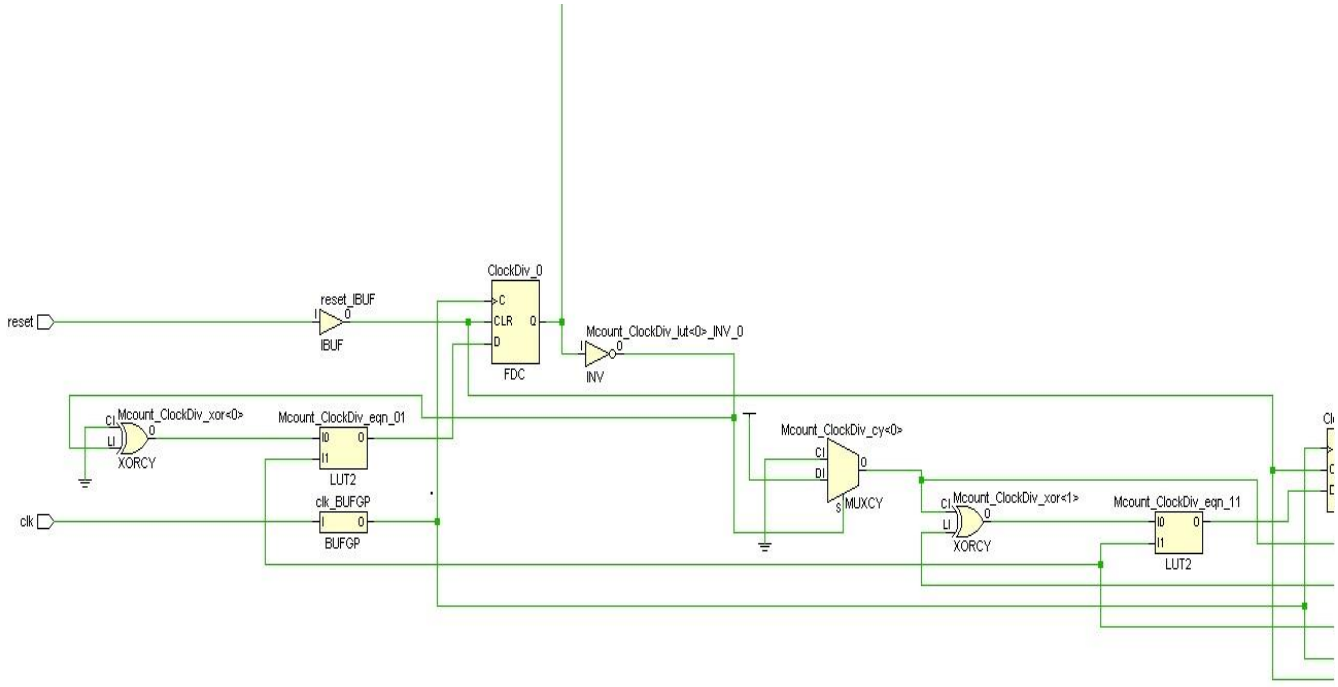

Fig. 14. Clock dividend section implements for SRAM cell

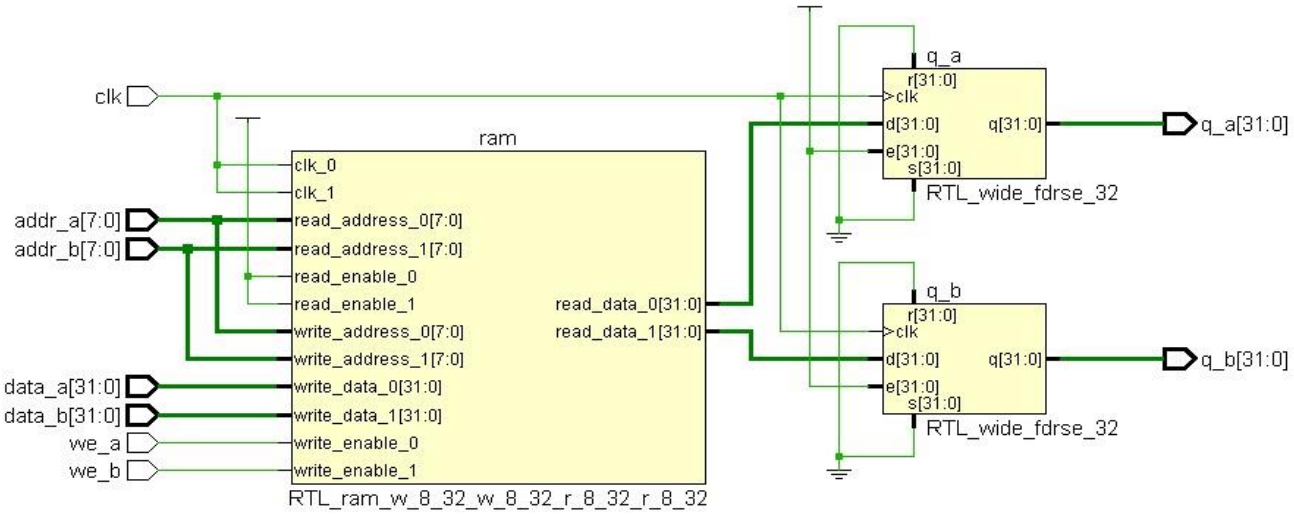

Fig. 15. Clock implemented SRAM Design

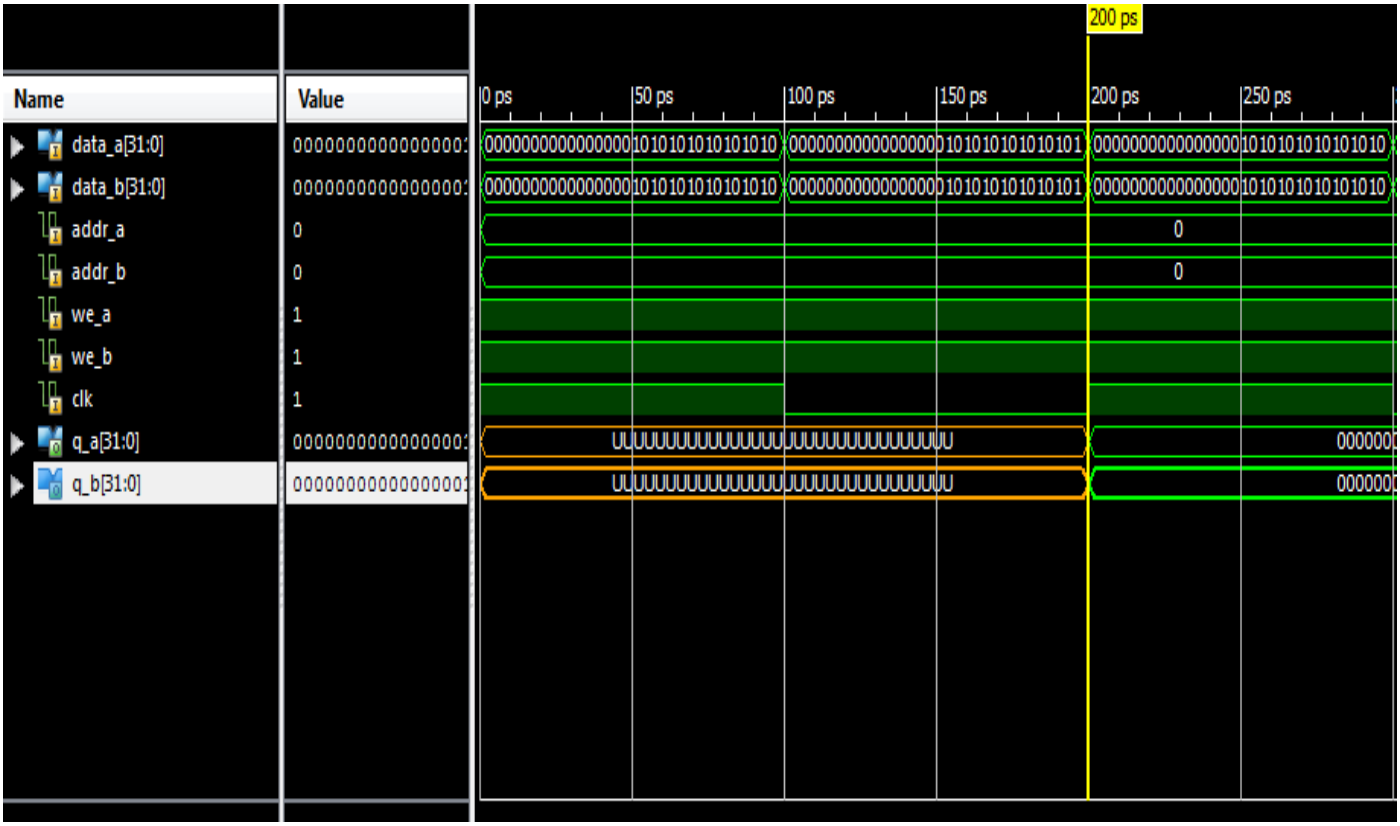

Fig. 16. Clock Implemented Memory Simulation

Propagation delay provides the maximum delay between a change in the input and the correct value appearing in the output state. Setup and hold time is the minimize duration that the data input to a flip-flops has to be at the desired value appear in before and after the relevant clock edge. A propagation delay time of clock implemented SRAM cell performs efficient simulation accessing between inputs to output states [Fig. 16]. If we implement data transitions according to the positive and negative edges of clocks then we get efficient results. We have analyzed the access time with various memories architecture [Fig. 17].

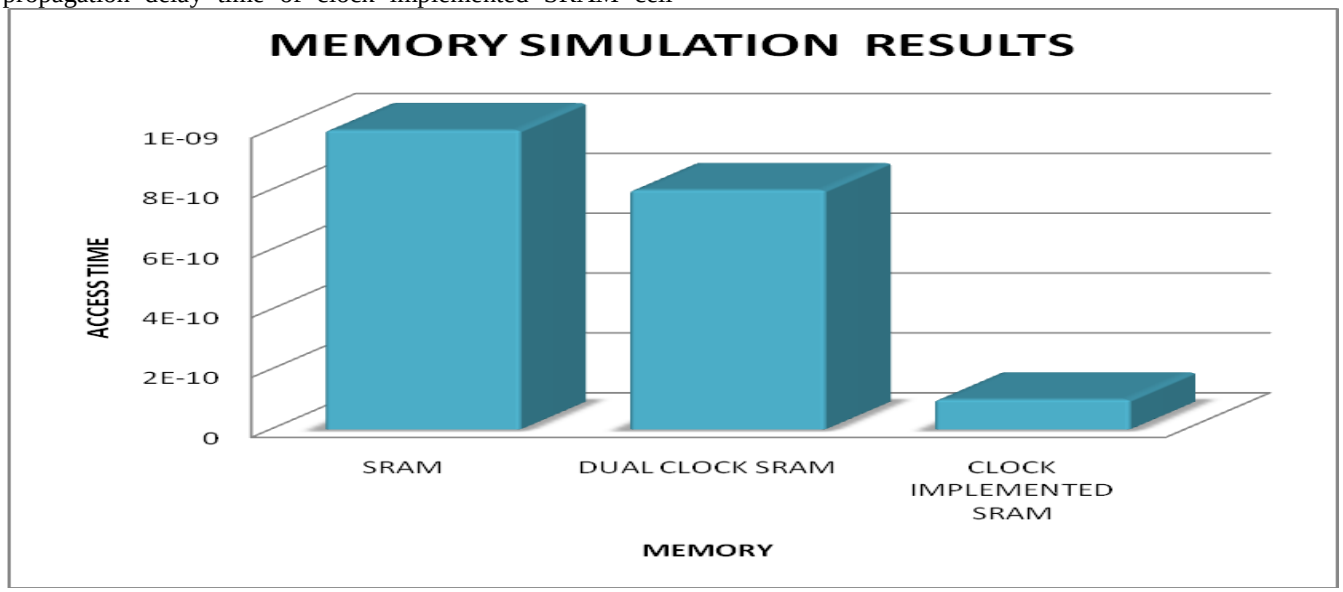

Fig. 17. Clock Implemented SRAM analysis

IV. Application Specific Memory Simulation

Clock implemented memory design have used according to our specific application. We have used standard Dhrystone application on target hardware environment and analyzed the ISA simulation behaviour with integrated Clock implemented memory design [Fig. 18]. Application specific ISA designs analyzed with XUP-5 FPGA hardware environments. These ISA designs implement processing behavior of our application. Clock implemented memory design analyzed for various ASIP simulation and low power consumption design architecture. Clock implemented memory architecture implements multiple data transitions scheme and implements simulation performance in efficient manner.

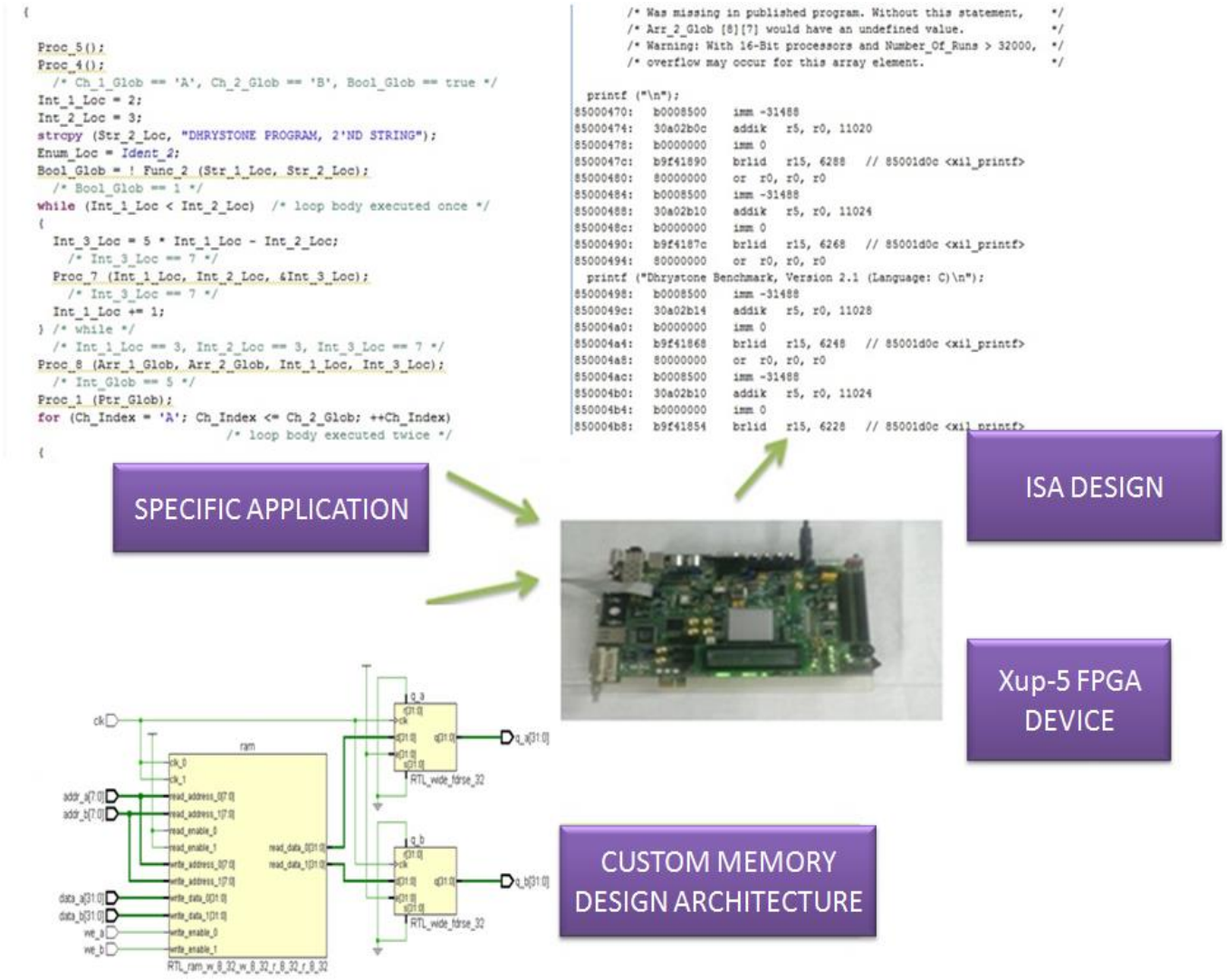

Fig. 18. Clock Implemented Application Specific Architectural Memory Design Simulation

V. Conclusion

Custom Cache architecture behaviour and it's efficiency analyzed with various simulators. Our main focus in this paper is to analyze the simulation efficiency of SRAM and analyzed internal clock architecture behaviour. In this paper we have analyzed Semiconductor material implemented memory design that improves internal efficiency of SRAM and reduces access time and propagation delay. Clock implemented architectural memory design implemented with clock subdivision mechanism and clock implemented memory designs implement multiple data transitions scheme that reduces meta-stability and data losses of SRAM.We have analyzed that memory performance depends upon row/column based architecture design and application specific access pattern.Clock implemented architectural memory design implements for ASIP design analysis.

Acknowledgment

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References

[1] M. Kuldar, K. Fan, M. Chu and S. Mahlke, "Automatic Synthesis of Customized Local Memories for Multiclustered Application Accelerators," IEEE 15th Int. Con. on Application Specific Systems, Architectures and Processors,2004, pp.304-314.

[2] P. Merolla, J. Arthur, F. Akopyan, N. Imam, R. Manohar and D.S. Modha, "A Digital Nero synaptic Core Using Embedded Memory with 45PJ per spike in 45nm," In Proc. of CICC, 2011,pp.25-32.

[3] P. R Panda, N. D. Dutt and A. Nicoulau, "Data Memory Organization and Optimization in Application Specific Systems," IEEE design & Tests of Computers,2001,pp.56-68.

[4] J. Park and P. C. Diniz, "Synthesis and Estimation of memory interfaces for FPGA-based Reconfigurable Computing Engines," In Pr. of FCCM'03, 2003,pp.297-299.

[5] F. Vahid, G. Stitt, Z. Guo and W. Najjar, "Technique for Synthesizing Binaries to an advanced Register/Memory Structure," In Pr. of *ACM* FPGA '05, 2005, USA.

[6] Xilinx tool Available on: http://www.xilinx.com/homepage/.

[7] B.S. Reniwal and S. K.Vishvakarma, "A Reliable, Process-Sensitive-Tolerant Hybrid Sense Amplifier for Ultralow Power SRAM,"Int. J. of Electronics and Electrical Engineering, vol. 1, no.1,2013,pp.34-38.

[8] Micro wind tool available on: http://www.microwind.net/.

[9] E. Ozer, R. Sendag and D. Gregg, "Multiple-Valued Caches for Power-Efficient Embedded Systems," In Pr. of.ISMVL'05, 2005.

[10] P. Wang, G. Sun, T. Wang, Y. Xie and J. Cong, "Designing Scratchpad Memory Architecture with Emerging STT-RAM Memory Technologies," In Pr. of ISCAS,2013, pp.1244-1247.

[11] B. H. Calhaun and A.P. Chandrkasan, "A 256-kb 65-nm Sub-threshold SRAM designs for ultra-low-voltage operation," Journal of solid-state circuits, vol.42, no. 3, 2007,pp. 680-688.

[12] K. Dhanumjaya, M. Sudha, M.N. Giri Prasad and K.Padmaraju, "Cell stability analysis of conventional 6t dynamic 8t SRAM cell in 45 nm technology," Int. J. of VLSI design & Communication Systems (VLSICS), vol.3, no.2, 2012, pp.41-51.

[13] G. Chen, D. Sylvester, D. Blauw and T. Mudge, "Yield-Driven Near-Threshold SRAM Design," IEEE Transactions on Very Large Scale Integration (VLSI) Systems,vol.18,no.11,2010,pp.1590-1598.

[14] N. K. Shukla, R.K. Singh and M. Pattanaik, "Design and Analysis of a Novel Low-Power SRAM Bit-Cell Structure at Deep-Sub-Micron CMOS Technology for Mobile Multimedia Applications," Int. J. of Advanced Computer Science and Applications,vol.2,no.5,2011,pp.43-49.

[15] A. K. Dadoria, A. S. Yadav and C.M. Roy, "Comparative Analysis of Variable N-T SRAM Cells," Int.J. of Advanced Research in Computer Science and Software Engineering,vol.3,no.4, 2013,pp.612-619.